A Drain Resistance Degradation Modeling Procedure of LDMOS's

Hitoshi Aoki[1,2*] and Masanori Shimasue[2]
1. Graduate School of Environmental Information, Teikyo Heisei University, Tokyo 164-8530, Japan
2. MoDeCH Inc., Tokyo 192-0081, Japan
* h.aoki@thu.ac.jp

Abstract— **A complete aging circuit simulation method using a drain resistance degradation model of laterally-diffused MOSFETs (LDMOS's) is presented. The drain resistance degradation caused by the hot electron injection (HCI) effect in the drain drift region has been formulated, and then implemented in SPICE. A practical circuit aging simulation procedure has been demonstrated with LDMOS measurements for a fundamental DC-DC converter circuit, effectively.**

Keywords— Reliability Simulation, Hot Carrier Injection, Aging Model, LDMOS, Compact Model

I. INTRODUCTION

Laterally diffused MOS (LDMOS) transistors are widely used in mixed-signal applications where high voltage capability is required. In typical applications these devices are switched between a state with high V_{ds} to low V_{gs} and a state with low V_{ds} to high V_{gs}. During switching, significant degradation induced by hot carrier injection (HCI) may occur [1]. Reliability circuit simulation needs to provide more accurate estimation of circuit lifetime than before. Several approaches [2-5] are reported, however, these are difficult for many circuit designers to follow the procedures because of their resource limitations. Among these approaches, [2] is relatively easy to apply for practical circuit design except that their peak electric field (E_m) calculation method is not described.

We derived the maximum electric field model by solving the Poisson equation using the LDMOS structure, and modify it with semi-empirical equations. Based on the new E_m model, a new drain drift region resistance (R_{drift}) degradation model of n-channel LDMOS has been developed and verified with stress measurements. Also, a new procedure to simulate circuit reliability without any loop-back is presented.

As shown in Fig. 1, our aging circuit simulation method is simple and straight-forward. HiSIM-HV model [6] has been applied to simulate n-channel LDMOS devices for "fresh" characteristic. The "stress" device characteristic is simulated by implementing our R_{drift} degradation model since R_{drift} is existing in the HiSIM-HV model as an internal variable. We define a switch parameter to enable/disable the degradation model. Static bias and temperature stress measurements are used for aging model parameter extractions, and RMS voltage biases are calculated from pulsed signals for transient stress simulations.

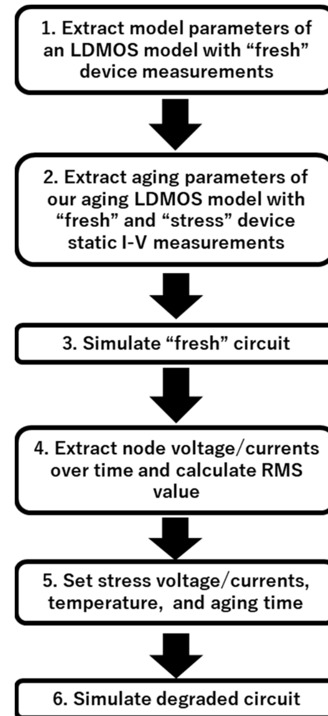

Fig. 1 Schematic illustration of the simulation flow used in circuit reliability simulation.

A fundamental DC-DC converter type test circuit is designed for our LDMOS degradation model verification. The circuit includes minimum number of passive components and one n-channel LDMOS to observe our model behavior.

II. HCI INDUCED DRAIN RESISTANCE DEGRADATION MODEL IN THE DRIFT REGION

The HCI degradation of n-channel LDMOS is to increase R_{drift} by decreasing carriers in the drift region [2]. The increased amount of R_{drift} correlates with the lateral maximum electric field. R_{drift} degradation model depends on time, which is written in the following equation [2]:

$$\frac{\Delta R_{drift}}{R_{drift}} = A_1 \cdot \ln\left(1+\frac{t}{\tau}\right) + A_2 \cdot \ln\left(1+\frac{t}{\gamma \cdot \tau}\right) \quad (1)$$

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where A_1, A_2, and γ are device specific parameters, t is the stressing time, τ is characteristic time which is a bias and geometry dependent parameter. In Eq. (1), τ is expressed in (2):

$$\tau = \left(\frac{\alpha \cdot W}{I_D}\right)^n \cdot \frac{\phi_b}{E_m \lambda} \, e^{\frac{\phi_b}{E_m \lambda}} \tag{2}$$

where α is a device specific empirical fitting parameter, W is the device width, E_m is the magnitude of the maximum electric field, n is a coefficient to be used for recent nano-meter process devices, λ is the mean free path that carriers can travel in this electric field before going through an energy losing scattering event, and ϕ_b is the energy needed for electrons to surmount the Si-SiO$_2$ energy barrier.

Since the stress bias voltages dependencies of V_{gs} and V_{ds} on the peak electric field should be supported, we developed physically based maximum electric field model equations. We have applied the LDMOS of maximum electric field model which is physically derived by solving the Poisson equation using the LDMOS structure in Fig. 2. The model is written as

$$E_m \equiv \left| -\frac{\partial \phi_f(0)}{\partial x} \right| = \sqrt{\alpha}\,\frac{\left(-\frac{\beta}{\alpha} + \phi_0\right)\cosh\left(\sqrt{\alpha}L\right) + \left(V_{ds} + \frac{\beta}{\alpha}\right)}{\sinh \sqrt{\alpha}L} \tag{3}$$

where α and β are described by the following equations.

$$\alpha = \frac{\varepsilon_0}{t_1 t_f \varepsilon_{si}} + \frac{2}{{t_1}^2} \tag{4}$$

and

$$\beta = -\frac{q}{\varepsilon_{si}}\left[N_d + N_{sub}\left(\frac{t_2}{t_1}\right)^2\right] \tag{5}$$

where t_1 is the epi layer thickness with a uniform doping concentration of N_d , t_2 is the substrate depletion layer thickness with doping concentration N_{sub}, t_f is the thickness of the front interface field oxide layer with the dielectric constant of ε_{ox}, x and y measure the horizontal and vertical positions relative to silicon surface, respectively.

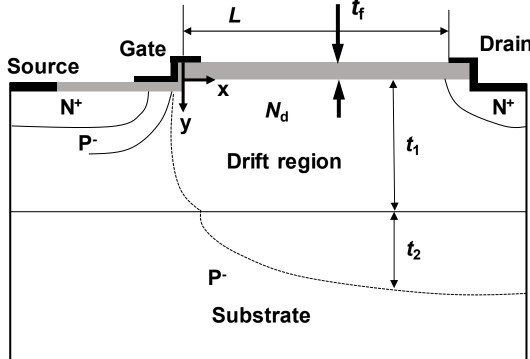

Fig.2 The structure of the n-channel LDMOS to derive the electric field.

The boundary conditions of the Poisson equation are expressed with Eq. (6).

$$\phi_f(0) = \phi_0 = 0\,, \phi_f(L) = V_{ds} \tag{6}$$

where ϕ_f is the surface potential function. The surface potential at $x = 0, \phi_0$, cannot be zero. It is expected to be a function dependent of V_{gs} and V_{ds}. However, if the function is defined as the surface potential, the differential equations cannot be solved, analytically. ϕ_0 is replaced with the empirical equation which includes the V_{gs} and V_{ds} dependencies at the boundary conditions.

The developed model is shown as

$$\phi_0 = d_1 \log\left(\frac{V_{ds}}{d_2}\right) - \left[1 - \exp\left(\frac{V_{gs} - V_{th}}{R}\right)\right] \tag{7}$$

where d_1, d_2, and R are fitting parameters.

III. SPICE Implementation and Experiments

Although we also implemented the threshold voltage degradation (ΔV_{th}) equation as

$$\Delta V_{th} = C_{HCI} * t^{\frac{1}{1+n_x}} \tag{8}$$

followed by DC HCI MOSFET model [7], it is negligibly small as shown in Fig. 3. Where C_{HCI} and n_x are fitting parameters.

We prepared an LDMOS whose gate oxide thickness, channel length, and channel width are 11.5 nm, 0.4 μm, and 500 μm, respectively, and then measured fresh and stressed I_{ds}-V_{gs}, I_{ds}-V_{ds} characteristics as shown in Figs. 3 and 4. Continuous gate and drain voltage stress has been supplied for 31,620 seconds at the temperature of 393 K. During the stressing process, the I-V measurements were performed, periodically as shown in Fig. 5. HiSIM model parameters are extracted with fresh DC I-V measurements in Figs. 3 and 4. Next, degradation parameters of our model are extracted with stressed and fresh DC I-V and I_{dmax} - time measurements in Figs. 3, 4 and 5. The degradation simulations as shown in these figures are accurate enough to estimate n-channel LDMOS characteristics.

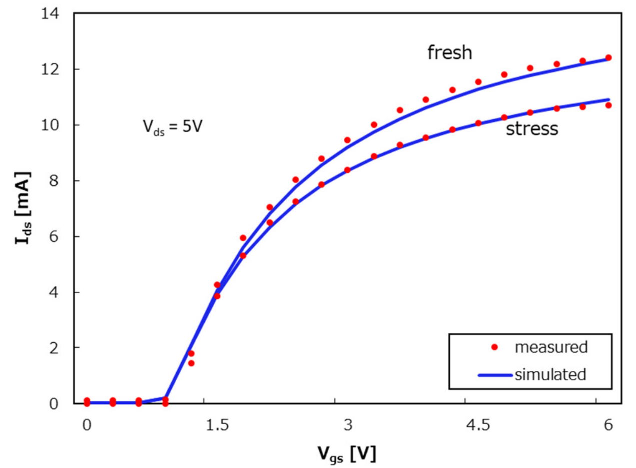

Fig.3 Fresh and stressed I_{ds} vs. V_{gs} characteristics of the n-channel LDMOS.

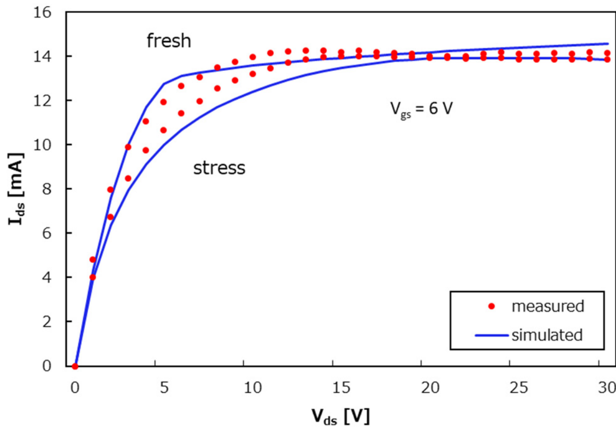

Fig.4 Fresh and stressed I_{ds} vs. V_{ds} characteristics of the n-channel LDMOS.

As shown in Fig. 4, the angle of the stressed simulation curve in the saturation region could be incorrect. Additional HiSIM-HV parameters need to be added and extracted for the correct simulations.

For a circuit verification, we organized a simple DC-DC converter as shown in Fig. 6. After the fresh simulation, the pulsed stress gate voltage of the n-channel LDMOS is monitored, and then calculate it to RMS value which is set to the stress gate voltage.

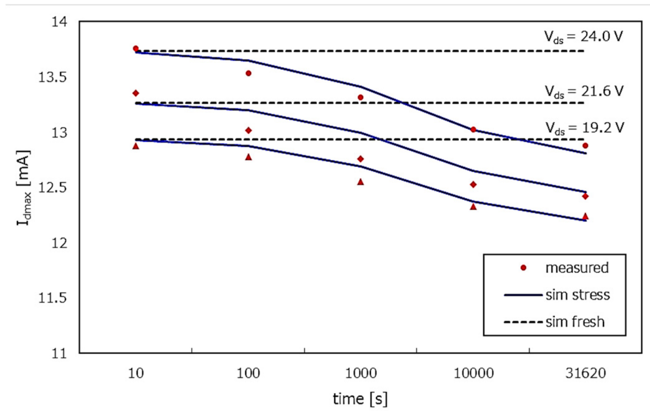

Fig.5 Fresh and stressed I_{dmax} vs. stressed time characteristics of the n-channel LDMOS. Where I_{dmax} is the drain current at V_{gs} = 6V.

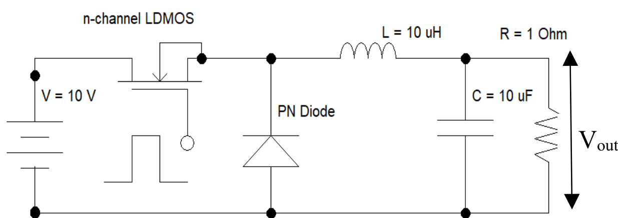

Fig.6 The equivalent test circuit of the fundamental DC-DC converter. A pulsed bias is supplied at the gate of the n-channel LDMOS device. The pulse period, rise time, fall time, delay time, width, and amplitude are 4.5 µs, 1 ns, 1 ns, 1ns, 2 µm, and 15 volts, respectively.

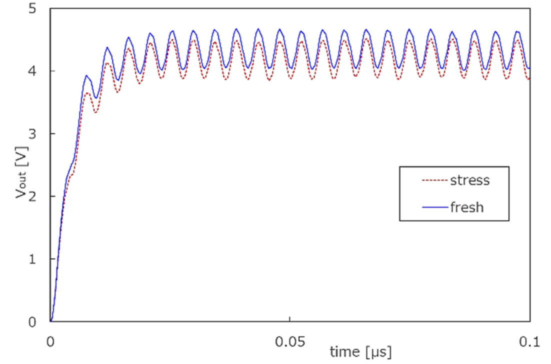

Fig. 7 Fresh and stressed V_{out} simulation waveforms of the test circuit (in Fig. 6).

The constant drain voltage of the n-channel LDMOS can be the stress drain voltage. After setting these two stress voltages, the stress simulation has been performed with the degradation model parameter is activated. The final stressed and fresh simulation results are shown in Fig. 7. The output voltage degradation is simulated, successfully.

IV. CONCLUSIONS

A new drain drift region resistance (R_{drift}) degradation model of n-channel LDMOS has been developed and verified with stress measurements. We derived the maximum electric field model by solving the Poisson equation using the LDMOS structure, and modified it with semi-empirical equations. The degradation model parameters of the model were extracted with n-channel LDMOS measurements, accurately.

Also, a new procedure to simulate circuit reliability without any loop-back is presented. Using the new model and the procedure, an aging simulation of a fundamental DC-DC converter was presented.

To complete the reliability modeling procedure to be applied for RF analog circuit designs AC and transient characterizations will be performed in the future research.

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